

Amendments to the Claims

Please cancel claim 6, amend claims 1-5, 7 and 8, and add new claims 11 and 12 as shown in the following list of claims. This listing of claims will replace
5 all prior versions, and listings, of claims in the application.

1 1. (currently amended) A memory device comprising, in a single integrated
2 circuit package:
3 a static memory means ~~(10, 12)~~ defining at least first and second nodes ~~(A,~~
4 ~~B)~~ communicatively connected with read and/or write data lines; and
5 at least one non-volatile memory means ~~(14, 16)~~ associated with said static
6 memory means ~~(10, 12)~~, and writing data stored therein to said static memory
7 means ~~(10, 12)~~; said non-volatile memory means comprising a first non-volatile
8 element ~~(14)~~ having a control gate connected to a first node ~~(B)~~ and a source
9 connected to a second node ~~(A)~~, and a second non-volatile element ~~(16)~~ having a
10 control gate connected to the second node ~~(A)~~ and a source connected to the first
11 node ~~(B)~~, the drain of each non-volatile element ~~(14, 16)~~ being connected by
12 means of a respective transistor ~~(18, 20)~~ to a supply means ~~(VDP)~~; characterized
13 in that said respective transistors are arranged to isolate the drains of the first and
14 second non-volatile elements from the supply means during a program cycle of
15 the memory device,
16 wherein the static memory means comprises a pair of cross-coupled
17 inverters.

1 2. (currently amended) A memory device according to claim 1, wherein said
2 non-volatile memory elements ~~(14, 16)~~ comprise embedded flash or EEPROM
3 elements.

1 3. (currently amended) A memory device according to claim 1, wherein said
2 non-volatile memory elements ~~(14, 16)~~ comprise double or single poly floating
3 gate type memory cells.

1 4. (currently amended) A memory device according to claim 1, wherein said
2 non-volatile memory elements (~~14, 16~~) comprise devices which can be
3 programmed and erased by means of tunneling of charges.

1 5. (currently amended) A memory device according to claim 1, wherein the
2 non-volatile memory elements (~~14, 16~~) are programmed with opposite data.

1 6. (canceled).

1 7. (currently amended) A memory device according to claim 1, wherein one
2 or more respective selection transistors (~~22~~) are provided, by means of which the
3 nodes (~~A, B~~) are communicatively coupled to the read and/or write lines.

1 8. (currently amended) A memory device according to claim 1, including one
2 or more isolation transistors (~~24~~).

1 9. (previously presented) A reconfigurable programmable logic device
2 including a memory device according to claim 1.

1 10. (previously presented) A field programmable gate array including a
2 memory device according to claim 1.

1 11. (new) A memory device according to claim 1, wherein gates of the
2 respective transistors are connected together to receive a common signal.

1 12. (new) A memory device according to claim 1, wherein each of the cross-
2 coupled inverters includes a pair of transistors, gates of the transistors of a first
3 inverter of the cross-coupled inverters being connected to the second non-volatile
4 element, gates of the transistors of a second inverter of the cross-coupled inverters
5 being connected to the first non-volatile element.